Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Appeal No.: 2006-2407

Application No.: 09/802,857 | Confirmation No.: 3304

Filed: March 12, 2001 | Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM | Examiner: M. J. Yigdall

REQUEST FOR RECONSIDERATION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Decision of the Board of Patent Appeals and Interferences ("the Board") mailed on October 31, 2006.

The Final Office Action of November 19, 2004 includes a rejection of claims 13-25 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,701,506 to Hosotani.

The Board concluded that the Examiner had made a *prima facie* case of obviousness and, thus, sustained the rejection of claims 13-25 under 35 U.S.C. §103.

For the following reasons, it is believed that there is insufficient evidence to support this result. Accordingly we suggest the filing of a Request For Rehearing. A Request For Rehearing is limited to points and authorities believed to have been misapprehended or overlooked in the Decision. 37 C.F.R. §41.52.

The Federal Circuit instructs that the Board is required to set forth in its opinions specific findings of fact and conclusions of law adequate to form a basis for appellate review. *Gechter v. Davidson*, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997) (Decision of the Board vacated and remanded for specific findings of fact and conclusions of law adequate to form a basis for appellate review).

Claim 13 - Claim 13 is drawn to a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a program memory storing a program, the data processing apparatus comprising:

a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits,

one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory,

one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide,

another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory,

another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide; and

a central processing unit receiving said plurality of coincidence signals, wherein said central processing unit:

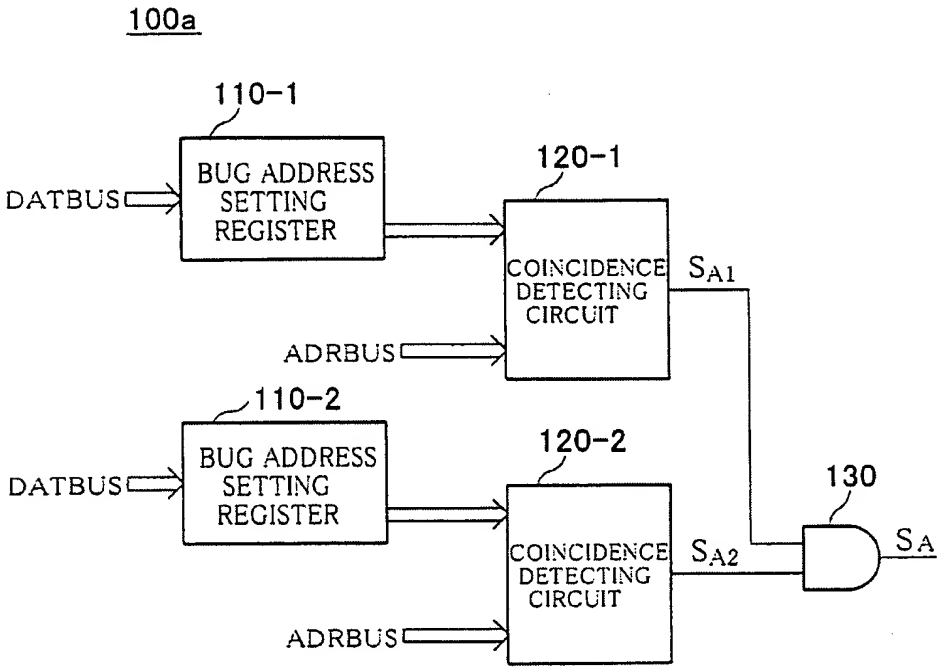
executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses,

executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses, and

executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses.

Figure 7 of the specification as originally filed is provided hereinbelow for the convenience of the Board. Figure 7 is block diagram of a second embodiment of the data processing apparatus according to the present invention and showing the configuration of the debugging circuit.

FIG.7



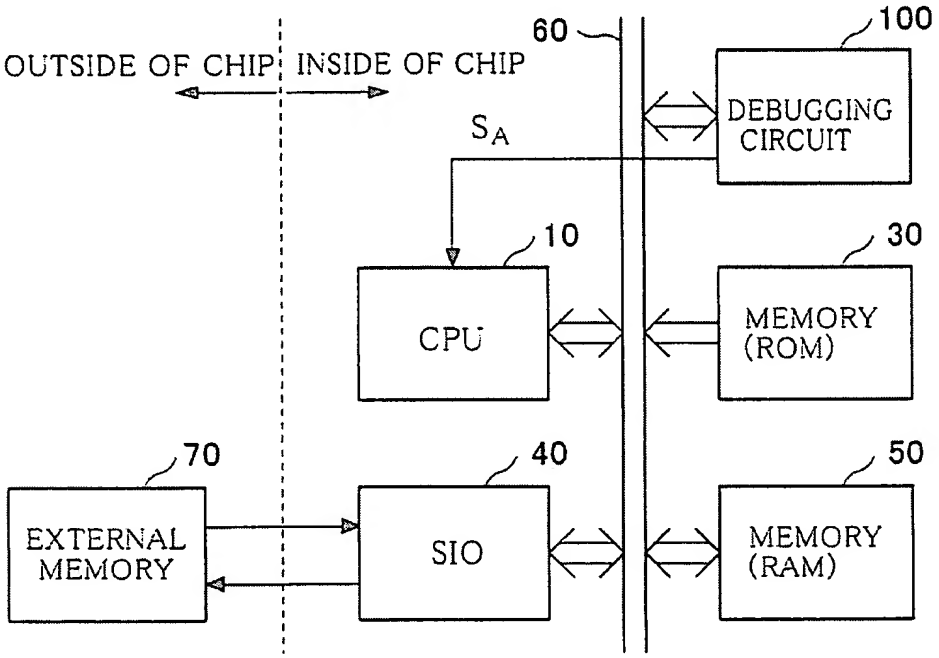
Claim 13 provides for one of *the plurality of coincidence detecting circuits* (120-1, 120-2) *outputting one of the plurality of coincidence signals* (S_{A1}, S_{A2}) when the program address and one of the plurality of bug addresses (BADR0-1, BADR0-2) coincide (Specification at page 24, lines 21-24).

Claim 13 additionally provides for *another of the plurality of coincidence detecting circuits* (120-1, 120-2) *outputting another of the plurality of coincidence signals* (S_{A1}, S_{A2}) when the program address and another of the plurality of bug addresses (BADR0-1, BADR0-2) coincide (Specification at page 24, lines 21-24).

In the data processing apparatus of the second embodiment shown in Figure 7, the parts other than the debugging circuit are *substantially the same as those in the first embodiment* (Specification at page 24, lines 5-7).

Figure 3 of the specification as originally filed is provided hereinbelow for the convenience of the Board. Figure 3 is block diagram of a first embodiment of the data processing apparatus according to the present invention.

FIG.3



Claim 13 further provides for *a central processing unit (10) receiving the plurality of coincidence signals* ($S_{A1, A2}$) (Specification at page 25, lines 4-6). In this case, as shown in Figure 7, the output signals (S_{A1}, S_{A2}) of the coincidence detecting circuits (120-1, 120-2) are input to an AND gate (130), and ***the output signal (S_A) of the AND gate (130) is input to the CPU 10 as the interrupt request signal*** (Specification at page 25, lines 10-14).

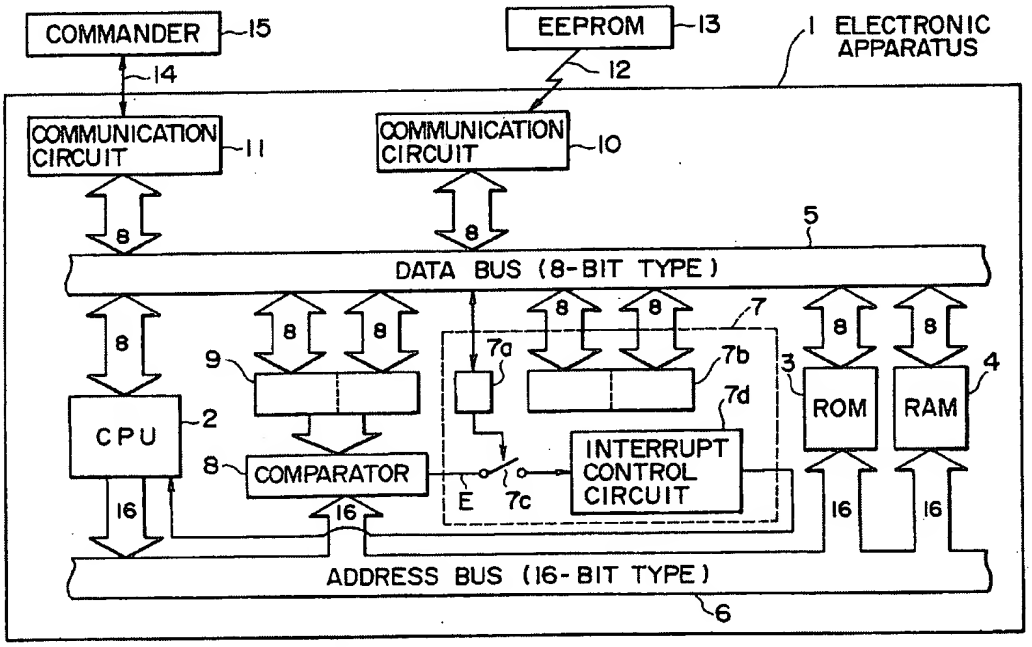
Sagane - first embodiment

- *The Decision on Appeal contends that Sagane would effectively receive the plurality of coincidence signals "as" a single or plural/separate interrupts, since Sagane has the capability to perform both according to the modified teachings of figure 3 to accommodate plural bugs (Decision on Appeal at page 7).*

In response, while this passage of the Decision on Appeal asserts that "Sagane would effectively receive the plurality of coincidence signals", the passage *fails* to assert that it is "***the CPU 2*** of Sagane that would effectively receive the plurality of coincidence signals".

Figure 1 of Sagane is provided hereinbelow for the convenience of the Board. Figure 1 of Sagane is a block diagram of an electronic apparatus practiced as a first embodiment of the invention.

FIG. 1



For the first embodiment of Sagane, Figure 1 of Sagane provides an **express** teaching of a ***coincidence signal E*** (Sagane at column 5, lines 14-15). While Sagane may teach the presence of a coincidence signal, Sagane ***fails*** to teach the coincidence signal E being received by the CPU 2.

Sagane provides that a switch 7c is opened when the control flag latch 7a is set to "0" and is closed when the latch 7a is set to "1"l (Sagane at column 3, lines 57-59).

The coincidence signal E enters an interrupt control circuit 7d as an interrupt request signal (Sagane at column 3, lines 57-61).

However, the Decision on Appeal fails to show in Figure 1 of Sagane that the CPU 2 receives the coincidence signal E.

This point, as argued in the Appellant's Brief at page 8, line 23 through page 11, line 26, is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

Additionally, while the first embodiment of Sagane may arguably depict some sort of linkage between the CPU 2 and the interrupt control circuit 7d (Sagane at figure 1), and while the first embodiment of Sagane arguably teaches that the interrupt handling effected by the interrupt control circuit 7d transfers control to the address given by an interrupt vector register 7b (Sagane at column 3, lines 61-63), *the first embodiment of Sagane **fails** to disclose, teach or suggest that an interrupt signal is provided from the interrupt control circuit 7d to the CPU 2* (Appellant's Brief at page 9, line 23 through page 10, line 4).

This point is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

Upon ***receipt of the command from the commander 15***, the CPU 2 of Sagane inhibits two kinds of write operations: the writing of the correction address from the EEPROM 13 to the interrupt generating address register 9, and the writing of the start address of the correction content

in the RAM 4 to the *interrupt vector register 7b* (Sagane at column 4, lines 16-21). The CPU 2 then sets the control flag latch 7a to "0" (Sagane at column 4, lines 21-23).

Yet, the command from the commander 15 of Sagane has not been shown to have been generated by a coincidence detecting circuit.

This point, as argued in the Appellant's Brief at page 9, line 23, through page 10, line 19, is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

- *Sagane further provides that, with the interrupt generated, control is passed on to the address latched in the interrupt vector register 7b, i.e., the start address of the correction content in the RAM 4 (step S9), and this causes the correction content (program) stored in the RAM 4 to be executed (step S10) (Sagane at column 5, lines 17-21).*

However, the Decision on Appeal fails to show the CPU 2 of Sagane as transferring control to the address given by an interrupt vector register 7b.

Instead, Sagane teaches that the interrupt handling effected *by the interrupt control circuit 7d* transfers control to the address given by an interrupt vector register 7b (Sagane at column 3, lines 61-63).

This point, as argued in the Appellant's Brief at page 9, line 12 through page 11, line 26, is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

Sagane - second embodiment

- *Page 8 of the Final Office Action includes an **admission** by the Examiner that the **second embodiment** of Sagane **fails** to disclose, teach or suggest the CPU 2 as receiving said plurality of coincidence signals.*

- *Page 6 of the Decision on Appeal concludes that in Sagane, the duplicated structural elements noted earlier would perform a sequential execution of a plurality of debugging programs upon the respective coincidence signals detected by the plural comparators by their issuance of the **coincidence or matching signal A** in figure 3.*

- *Page 7 of the Decision on Appeal asserts that because the CPU 2 in figure 3 of Sagane would effectively bypass its normal program sequencing to eliminate the program bug within its nominal programming in ROM 3 upon the normal operation of the plurality comparators 8 in figure 3, the effect of the operation of the system in figure 3 is to function in a manner analogous to an interrupt as directly taught in the embodiment in figure 1 of Sagane.*

- *Page 7 of the Decision on Appeal further concludes that, in this manner, the functional analogy of Sagane is consistent with the broad recitation of dependent claims 19 and 20 that Sagane would effectively receive the plurality of coincidence signals "as" a single or plural/separate interrupts, since Sagane has the capability to perform both according to the modified teachings of figure 3 to accommodate plural bugs.*

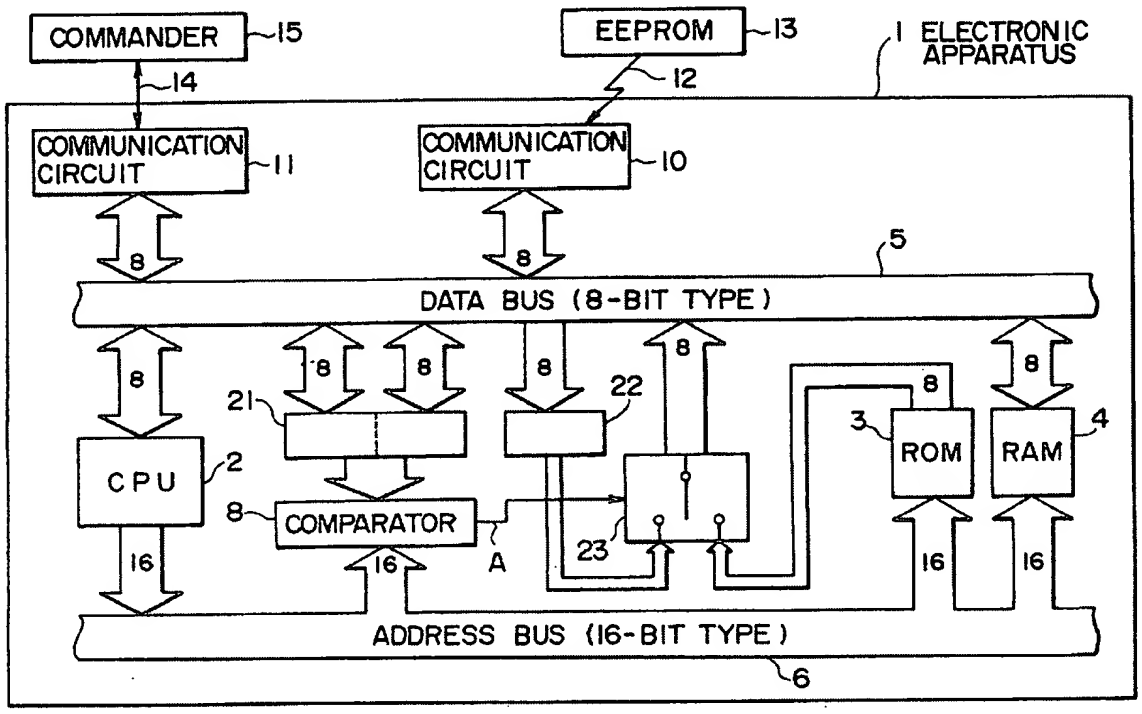
In response, nowhere within Sagane is there found a disclosure, teaching or suggestion that the *interrupt control circuit 7d* of Figure 1 corresponds with the *switch 23* of Figure 3 (Reply Brief at page 4, lines 9-10). Whereas Figure 1 arguably depicts a link between the interrupt control circuit 7d and the CPU 2, no such link is found within Figure 3 of Sagane between the switch 23 and the CPU 2 (Reply Brief at page 4, lines 10-12).

As shown hereinabove, Figures 3 and 7 of the Appellant's specification as originally filed provide that ***the output signal (S_A) of the AND gate (130) is input to the CPU 10 as the interrupt request signal*** (Specification at page 25, lines 10-14).

Conversely, *no interrupt signal of any type* is shown within Figure 3 of Sagane to reach the CPU 2.

Specifically, Figure 3 of Sagane is provided hereinbelow for the convenience of the Board. Figure 3 of Sagane is a block diagram of an electronic apparatus practiced as a second embodiment of the invention.

FIG. 3



However, the Decision on Appeal has failed to show that the second embodiment of Sagane teaches the CPU 2 has received the coincidence or matching signal A. In fact, Figure 3 of Sagane depicts a signal A being applied to a switch 23 and NOT to the CPU 2.

Yet, signal A, as shown within Figure 3 of Sagane, ***NEVER*** reaches the CPU 2.

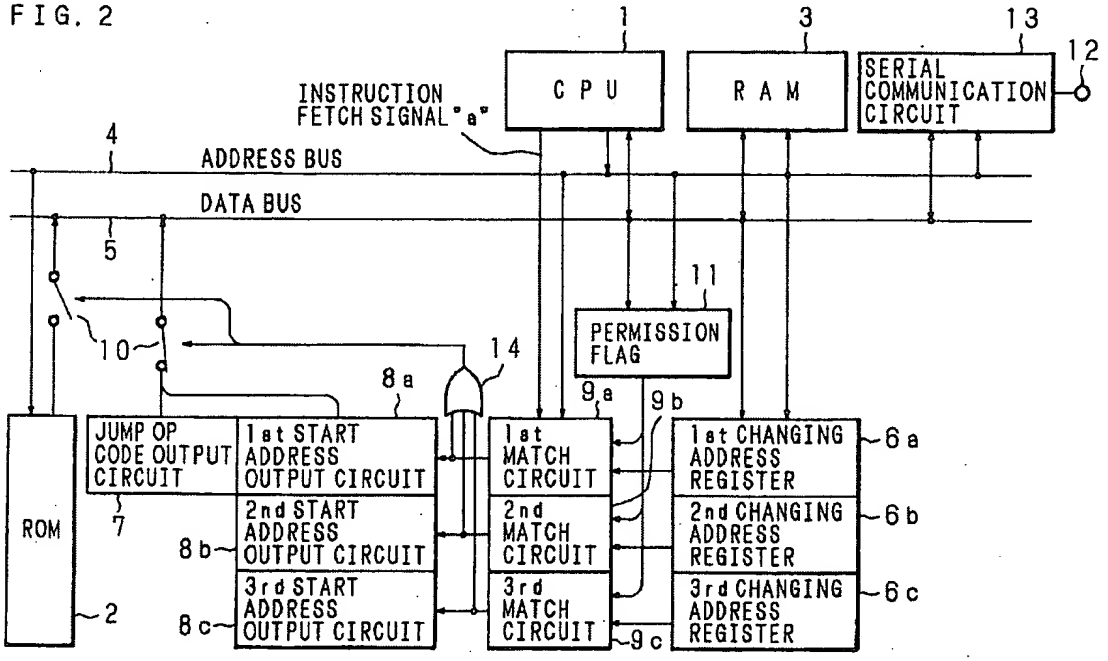
This point is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

Hosotani

- *Regarding Hosotani, page 8 of the Decision on Appeal asserts that the operation of the OR gate in these figures which results from a match circuit/coincidence circuit output from sub-circuits 9a- 9c, as well as the operation of the switch/connection control 10, provides a selective output from one or plurality of bugs detected to the data bus 5 which feeds directly to the CPU 1 in figure 2, for example, of Hosotani.*

The Examiner's Answer of February 6, 2006 refers to Figure 2 of Hosotani (Examiner's Answer at page 7). Figure 2 of Hosotani is provided hereinbelow for the convenience of the Board. Figure 2 of Hosotani is a block diagram showing the configuration of a microcomputer, having a ROM program alterability, according to a first embodiment of the present invention.

FIG. 2



Hosotani arguably teaches the presence of an OR circuit 14 and a connection control means 10. ***However, the Decision on Appeal has failed to show that Hosotani teaches the output of the OR circuit 14 being received by the CPU.***

Instead, Hosotani teaches that the *output of the OR circuit 14 is connected to a connection control means 10* (Hosotani at Figures 2).

The *output of the OR circuit 14 is connected to a connection control means 10* which selects either the mask ROM 2 or a jump op code output circuit 7 and first to third start address output circuits 8a-8c for connection to the data bus 5 in accordance with the output level of the OR circuit 14 (which outputs a "1" level when the result of comparison from any one of the match circuits 9a-9c indicates a match, and a "0" level when all the comparison results indicate a mismatch) (Hosotani at column 4, line 61 to column 5, line 2).

This point is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

Direct connection or a direct coupling

- *The Decision on Appeal, on page 7, asserts that the mere reception of the coincidence signals by the CPU of claim 13 does not require explicitly a direct connection or a direct coupling.*

In response to this assertion, while it is agreed that the mere reception of the coincidence signals by the CPU of claim 13 does not require explicitly a direct connection or a direct coupling, claim 13 does provide for the central processing unit *receiving* said plurality of coincidence signals. The express language of claim 13 is unambiguous.

Nowhere within the express language of claim 13 is there found that the central processing unit receives "*the effect of*" the plurality of coincidence signals. Instead, the express language of claim 13 provides that the plurality of coincidence signals, themselves, is received by the central processing unit.

However, the Decision on Appeal fails to show in the actual receipt of a coincidence signal, directly or indirectly, by the CPU of either Sagane or Hosotani.

This point is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

In conclusion, the ***absence*** of the central processing unit receiving a coincidence signal that has been outputted by a coincidence detecting circuit is point is believed to have been misapprehended or overlooked by the Board in rendering its Decision.

The previously stated points are believed to have been misapprehended or overlooked in the Decision of the Board mailed on October 31, 2006 and are grounds upon which rehearing is sought.

Accordingly, the Board is respectfully requested to reconsider its Decision in this regard.

Dated: December 29, 2006

Respectfully submitted,

By_____
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